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	AC						
OTHER DOCUMENTS							
DF	AD	G. Croft et al., <i>ESD Protection Techniques for High Frequency Integrated Circuits</i> , Microelectronics Reliability 38, 1998, pp. 1681-1689.					
DF	AE	J. Z. Chen et al., <i>Design and Layout of a High ESD Performance NPN Structure for Submicron BiCMOS-Bipolar Circuits</i> , 34th Annual IEEE International Reliability Physics Symposium Proceedings, 1996, pp. 227-232.					
DF	AF	J.C. Bernieret et al., <i>A Process Independent ESD Design Methodology</i> , IEEE International Symposium on Circuits and Systems Proceedings 1, 1999, pp. 218-221.					
DF	AG	W.D. Mack et al., <i>New ESD Protection Schemes for BiCMOS Processes with Application to Cellular Radio Designs</i> , IEEE International Symposium on Circuits and Systems 6, 1992, pp. 2699-2702.					
Examiner		Date Considered					
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